ABSTRACT OF THE DISCLOSURE

A compact dynamic random access memory (DRAM) cell and highly efficient methods for using the DRAM cell are disclosed. The DRAM cell provides reading, writing, and storage of a data bit on an ASIC chip. The DRAM cell includes a first transistor acting as a pass gate and having a first source node, a first gate node, and a first drain node. The DRAM cell also includes a second transistor acting as a storage device and having a second drain node that is electrically connected to the first drain node to form a storage node. The second transistor also includes a second source node and a second gate node. The second source node is electrically floating, thus increasing the effective storage capacitance of the storage node.